Worksheet 1B Processor components Answers

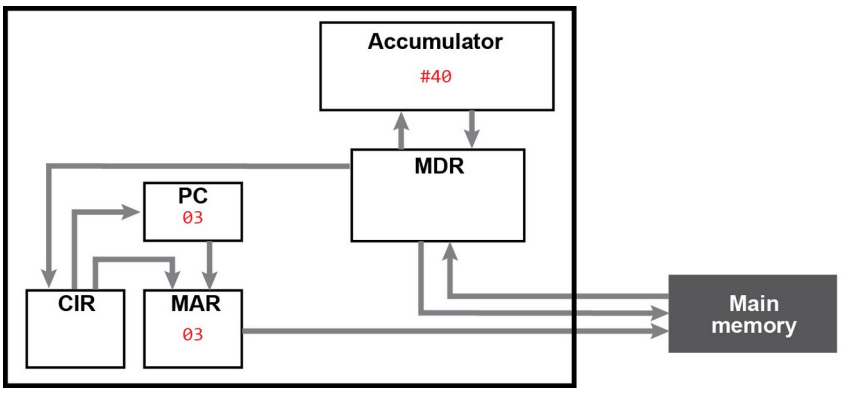
1. A computer is designed to be programmed using simplified assembly language. The instruction in memory location `03` is `ADD 06` and is used to add the value stored in memory location `06` to the value stored in the accumulator.

   Numerical values are being used and are labelled with a # mark. The value currently in the accumulator is `#40`. There is a value of `#15` in memory location `06`.

   Complete the diagrams of the states of the processor components at various stages in the Fetch-Execute cycles showing how the result of this instruction is determined and stored in the accumulator.

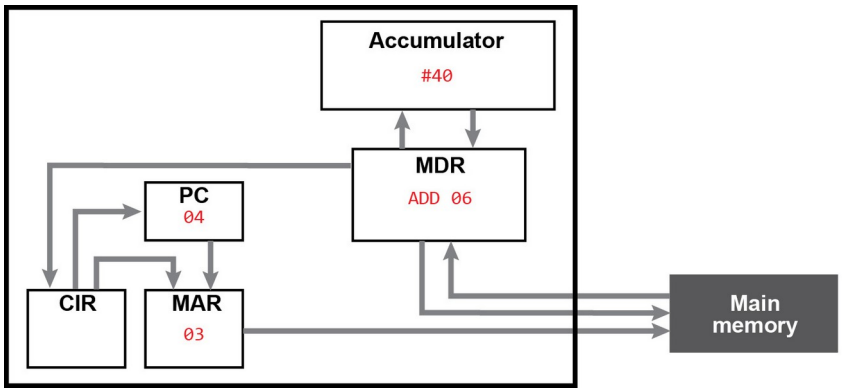
   Also add to the diagram a description of what is happening at each part of the three main stages, (the first has been completed as an example):

Fetch – Stage 1



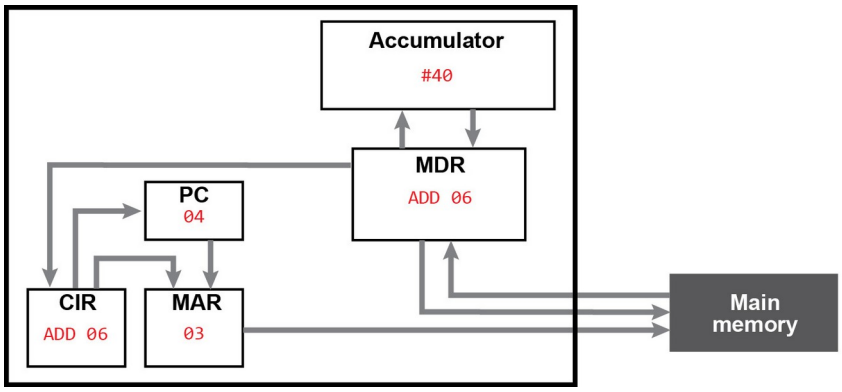
Description of diagram:
The Program Counter contains the memory address of the next instruction to be processed, (03). This is copied into the Memory Address Register so that the instruction can be read. A request is sent to main memory to copy the contents of this address into the MDR.

Fetch – Stage 2



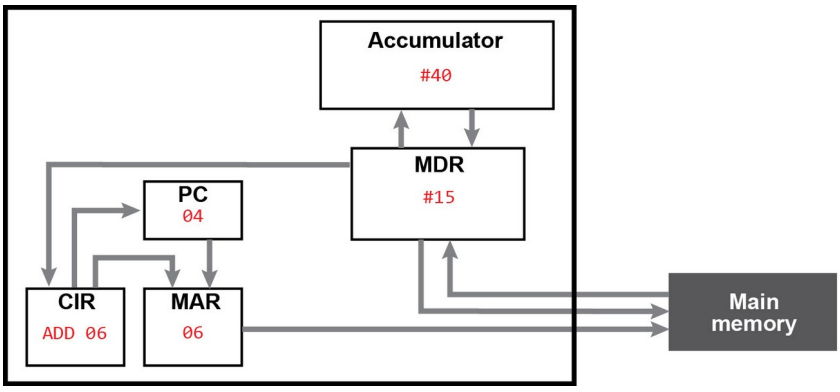
Description of diagram:
The instruction stored in address 03 is placed on the data bus and read into the Memory Data Register and the Program Counter is incremented by 1.

Fetch – Stage 3



Description of diagram:
This instruction is copied from the Memory Data Register into the Current Instruction Register.

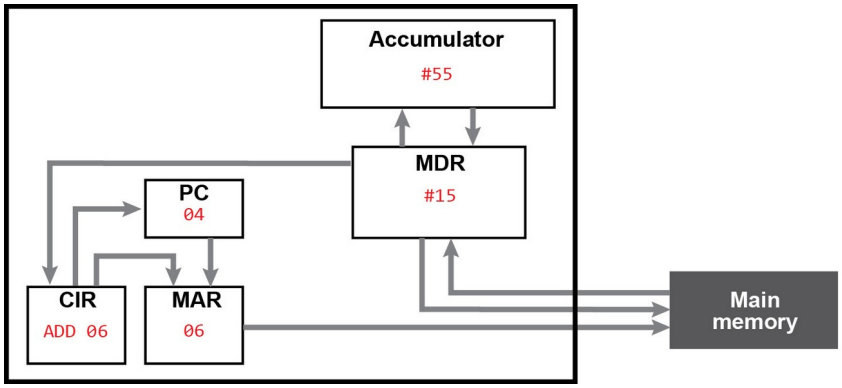
Decode – Stage 4



Description of diagram:

The instruction in the CIR is decoded by the Control Unit. Operands in memory are required so the address of the operand is copied into the MAR. The data stored in address 06 is placed on the data bus and read into the Memory Data Register.

Execute – Stage 5



Description of diagram:
The instruction is carried out and the result of the instruction is left in the accumulator.

2. The next instruction at address `04` is `STA 07` which stores the result of the previous instruction in memory location `07`. Describe broadly the process the Fetch-Execute cycle will follow to achieve this.

The stages are:

- Contents of PC copied to MAR
- Instruction fetched from memory location and placed in MDR
- PC incremented by one
- Instruction stored in the CIR
- Instruction decoded by the Control Unit
- Operand (07) copied to MAR
- Value in accumulator (55) copied to MDR
- Address (07) from instruction used by MAR
- Value 55 written to memory location 07

You can try out a simulation of this process on the LMC (Little Man Computer), entering the Assembly code

```
          INP
          STA first
          INP
          ADD first
          STA second
          HLT
first     DAT
second    DAT
```

Run the program entering the values 15 and 40.

The Little Man Computer http://peterhigginson.co.uk/LMC/